FLASH ADCS
FLASH ADC ARCHITECTURE

- Reference ladder consists of $2^N$ matched resistors
- Input is compared to $2^N-1$ reference voltages
- Massive parallelism
- Very fast ADC architecture
- Latency = $1 \ T_s = 1/f_s$
- Throughput = $f_s$
- Complexity = $2^N$

Diagram showing a ladder of resistors and comparators with input $V_i$, reference voltage $V_{FS}$, strobe signal, and output $D_{out}$. The diagram includes $2^{N-1}$ comparators.
THERMOMETER CODE

- Voltage sources: $V_{FS}$ and $V_i$
- Strobe signal: $f_s$
- $2^{N-1}$ comparators

Diagram:
- Comparator outputs: 0, 1, 1
- Thermometer code
- Digital Backend
- Binary Code
- Output: $D_{out}$
THERMOMETER CODE

Thermometer code

2^{N-1} comparators

1-of-n code

ROM encoder

V_{FS} V_i

Strobe

f_s

b_2 b_1 b_0

111

110

010

001

000

V_{FS} V_i

f_s

Strobe

comparators

Thermometer code

1-of-n code

ROM encoder
FLASH ADC CHALLENGES: EXAMPLE

- $V_{DD} = 1.8$ V
- 10-bit
- $V_{FS} = 1$ V
- DNL < 0.5 LSB
- $0.5$ mV = 3-5 $\sigma$ → 1 LSB = 1 mV
- $V_{os}$ < 0.5 LSB
- $\sigma = 0.1$-0.2 mV

- $2^N$-1 very large comparators
- Large area, large power consumption
- Very sensitive design
- Limited to resolutions of 4-8 bits
FLASH ADC CHALLENGES

- DNL < 0.5 LSB
- Large Full-scale voltage (V_{FS}) relaxes offset tolerance
- Small V_{FS} benefits conversion speed (settling, linearity of building blocks)
ADC INPUT CAPACITANCE

\[ \sigma^2 (V_{th}) = \frac{A_{Vth}^2}{WL} \]

\[ C_g = 10 \text{ fF/\mu m}^2 \]

- **N** = 6 bits → 63 comparators
- **\( V_{FS} \)** = 1 V → 1 LSB = 16 mV
- **\( \sigma \)** = LSB/4 → \( \sigma \) = 4 mV
- **\( A_{VT0} \)** = 10 mV·\( \mu \)m → \( L = 0.24 \mu m, W = 26 \mu m \)

<table>
<thead>
<tr>
<th>N (bits)</th>
<th># of comp.</th>
<th>( C_{in} ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>63</td>
<td>3.9</td>
</tr>
<tr>
<td>8</td>
<td>255</td>
<td>250</td>
</tr>
<tr>
<td>10</td>
<td>1023</td>
<td>??!</td>
</tr>
</tbody>
</table>

- Small **\( V_{os} \)** leads to large device sizes, hence large area and power
- Large comparator leads to large input capacitance, difficult to drive and difficult to achieve sufficient tracking bandwidth

FULLY-DIFERENTIAL ARCHITECTURE

- $V_{FS}$ is effectively doubled
- 3-dB gain in SNR
- Better CMRR
- Noise immunity
- Input feedthrough is cancelled
- $C_{in}$ nonlinearity partially removed
FLASH ADC DESIGN CONSIDERATIONS

• Use a dedicated S/H (or T/H) for better dynamic performance
  – Can be avoided when using the A/D inside a ΔΣ loop

• Large input range for the quantizer has several benefits
  – Increased step-size ($V_{\text{LSB}}$) relaxes offset requirements on the comparators
  – Reduced matching requirements result in small input cap to the S/H, easier to drive
  – Reduced input cap results in smaller clock routing parasitics – power savings in clock drivers

• Comparator Design
  – See comparator design notes/slides
FLASH ADC: REFERENCE LADDER

• Differential reference ladder
• Decaps on the reference taps
  – large $RC$ time-constant will not allow reference restoration after kickback noise
  – Small $R$ will lead to power dissipation
  – Optimize $RC$ time-constant value
• Subtract references from the input in a differential manner
  – Several topologies are possible
• Several architectures for the digital backend
  – May need to pipeline digital logic at high sampling rates $>500$ MS/s
REFERENCE GENERATOR (FOR $V_{REFP}$ AND $V_{REFM}$)

[Brooks 1994]

External decoupling caps provide dynamic currents
⇒ Low power reference buffer
FLASH ADC: REFERENCE SUBTRACTION
REFERENCE SUBTRACTION: SCHEME I

- Employ reference ladder for subtraction
- Choose current ($I$) such that differential voltage drop across $R = 1\ V_{\text{LSB}}$
- Ladder is part of the signal path
  - Comparator input cap load the resistor taps
  - Excess delay

\[
A_{\text{max}} = \frac{0.5V_{\text{dd}} - \Delta V}{2}
\]

REFERENCE SUBTRACTION: SCHEME II

- Source followers to buffer $v_{in}$
  - reduced swing, varies with PVT
- Ladder is part of the signal path
  - Comparator input cap load the resistor taps
  - Excess delay

REFERENCE SUBTRACTION: SCHEME III

- Differential difference amplifier for subtracting the reference
  - followed by a zero crossing detector
- Relaxes the impedance requirements on the ladder
- Mismatch in differential pairs and tail current sources results in comparator offset
  - current trimming (see the reference below)
- Finite BW of the amplifier causes excess delay

REFERENCE SUBTRACTION: SCHEME IV

- Switched-capacitor reference subtraction
  - Pay attention to charge injection
- ADC can handle large input swing
- Slow when auto-zeroing preamp is used
  - Large settling time constant
  - Reference subtraction in background
EXAMPLE: FULLY-DIFFERENTIAL COMPARATOR

- Double-balanced, fully-differential preamp
- Switches (M₇, M₈) added to stop input propagation during regeneration
- Active pull-up PMOS added to the latch
FLASH ADC: ERRORS
FLASH ADC ERRORS

- SHA-less
- Signal and clock propagation delay
- $2^{N-1}$ PAs + latches must be matched
- Synchronized clock strobe signal is critical

Going parallel is fast, but also gives rise to inherent problems...
Input CM difference creates systematic mismatch (offset, gain, $C_{in}$, tracking BW, and CMRR) among preamps
**SAMPLING APERTURE ERROR**

- Preamp delay and $V_{THN}$ of sampling switch ($M_9$) are both signal-dependent → signal-dependent sampling point (aperture error)

- A major challenge of distributing clock signals across $2^N-1$ comparators in flash ADC with minimum clock skew (routing, $V_{THN}$ mismatch of $M_9$, etc.)
Signal-dependent input bandwidth \((1/R_S C_{in})\) introduces distortion
Feedthrough of $V_{in}$ to the reference ladder through the serial connection of $C_{gs1}$ and $C_{gs2}$ disturbs the reference voltages.
COMPARATOR METASTABILITY

- Cascade preamp stages (typical flash comparator has 2-3 PA stages)
- Use pipelined multi-stage latches; PA can be pipelined too
- Avoid branching off comparator logic outputs

Assuming that the input is uniformly distributed over $V_{FS}$, then

$$\text{BER} = \frac{\Delta}{1 \text{ LSB}}$$

$$V_o(t) = V_i(0) \cdot A_v1 A_v2 \cdot \exp(t \cdot g_m/C_L)$$
COMPARATOR METASTABILITY

Logic levels can be misinterpreted by digital gates (branching off, diff. outputs)
BUBBLES (SPARKLES) IN THERMOMETER CODE

Static/dynamic comparator errors cause bubbles in thermometer code.
Comparator offset

Timing error

BUBBLES (SPARKLES)
BUBBLE-TOLERANT BOUNDARY DETECTOR

- 3-input NAND
- Detect “011” instead of “01” only
- “Single” bubble correction
- Biased correction

Inspecting more neighboring comparator outputs improves performance
MAJORITY VOTING LOGIC

\[ C_j^- = C_{j-1}C_j + C_jC_{j+1} + C_{j-1}C_{j+1} \]

<table>
<thead>
<tr>
<th>Case</th>
<th>“011” Det.</th>
<th>Majority voting</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>③</td>
<td>②</td>
</tr>
<tr>
<td>B</td>
<td>Fail</td>
<td>②</td>
</tr>
<tr>
<td>C</td>
<td>②</td>
<td>②</td>
</tr>
<tr>
<td>D</td>
<td>Fail</td>
<td>Fail</td>
</tr>
</tbody>
</table>

GRAY ENCODING

\[ G_1 = T_1 T_3 + T_5 T_7 \]
\[ G_2 = T_2 \overline{T_6} \]
\[ G_3 = T_4 \]

Only one transition
b/t adjacent codes

<table>
<thead>
<tr>
<th>Thermometer</th>
<th>Gray</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0</td>
<td>0 0 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0</td>
<td>0 0 1</td>
<td>0 0 1</td>
</tr>
<tr>
<td>1 1 0 0 0 0 0</td>
<td>0 1 1</td>
<td>0 1 0</td>
</tr>
<tr>
<td>1 1 1 0 0 0 0</td>
<td>0 1 0</td>
<td>0 1 1</td>
</tr>
<tr>
<td>1 1 1 1 0 0 0</td>
<td>1 1 0</td>
<td>1 0 0</td>
</tr>
<tr>
<td>1 1 1 1 1 0 0</td>
<td>1 1 1</td>
<td>1 0 1</td>
</tr>
<tr>
<td>1 1 1 1 1 1 0</td>
<td>1 0 1</td>
<td>1 1 0</td>
</tr>
<tr>
<td>1 1 1 1 1 1 1</td>
<td>1 0 0</td>
<td>1 1 1</td>
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</table>

<table>
<thead>
<tr>
<th>T_1</th>
<th>T_2</th>
<th>T_3</th>
<th>T_4</th>
<th>T_5</th>
<th>T_6</th>
<th>T_7</th>
<th>G_3</th>
<th>G_2</th>
<th>G_1</th>
<th>B_3</th>
<th>B_2</th>
<th>B_1</th>
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<tbody>
<tr>
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</tr>
</tbody>
</table>

- One comparator output is ONLY used once \(\rightarrow\) No branching!
- Gray encoding fails benignly in the presence of bubbles
- Codes are also robust over metastability errors
Conversion of Gray code to binary code is quite time-consuming → “quasi” Gray code

<table>
<thead>
<tr>
<th>Thermometer</th>
<th>Gray</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0</td>
<td>1 0 1 1</td>
<td>13</td>
</tr>
<tr>
<td>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 0</td>
<td>1 0 0 0</td>
<td>15</td>
</tr>
<tr>
<td>1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 1</td>
<td>1 0 1 0</td>
<td>12</td>
</tr>
</tbody>
</table>

FLASH ADC: BINARY DECODERS
GRAY ENCODED ROM DECODER

Thermometer-to-Binary Decoders for Flash Analog-to-Digital Converters

Erik Ståhl and Mark Vesterbacka
WALLACE TREE ADDER (1st ADDER)

Wallace tree decoder for an $N = 4$-bit flash ADC.
FOLDED WALLACE TREE DECODER
MUX-BASED DECODER

Multiplexer-based decoder for $N = 4$ bits.
COMPARISON OF DECORDER SCHEMES

- Mostly custom design at higher speeds
- Pipeline the digital backend at high-sampling rates to meet clock timing
  - $T_{pd} < T_{CK} - (t_{pcq} + t_{setup})$
  - $T_{cd} > t_{hold} - t_{ccq}$
FLASH ADC: OTHER TECHNIQUES
OFFSET AVERAGING (1)

[Kattmann & Barrow, ISSCC 1991]
OFFSET AVERAGING (2)

[Bult & Buchwald, JSSC 12/1997]

[Scholtens & Vertregt, JSSC 12/2002]
FLASH ADC WITH AVERAGING

[Choi & Abidi, JSSC 12/2001]

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>6 bits</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>1.3 GS/s</td>
</tr>
<tr>
<td>INL/DNL @ Fs = 1 GHz</td>
<td>0.35 LSB / 0.2 LSB</td>
</tr>
<tr>
<td>Input Range</td>
<td>1.6 V_{pp} differential</td>
</tr>
<tr>
<td>Input Capacitance (T/H)</td>
<td>1 pF</td>
</tr>
<tr>
<td>Bit Error Rate @ fs = 1 GHz</td>
<td>$&lt; 10^{-10}$</td>
</tr>
<tr>
<td>SFDR @ fin = 100 MHz</td>
<td>&gt; 44 dB up to 1.3 GS/s</td>
</tr>
<tr>
<td>SNDR @ fin = 530 MHz</td>
<td>35 dB @ 1 GS/s</td>
</tr>
<tr>
<td>@ fin = 650 MHz</td>
<td>32 dB @ 1.3 GS/s</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>500 mW @ 1 GS/s</td>
</tr>
<tr>
<td>(56% due to logic and clock)</td>
<td>545 mW @ 1.3 GS/s</td>
</tr>
<tr>
<td>Voltage Supply</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Active/Total Die Area</td>
<td>2x0.4 mm² / 2.2x2.2 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35-μm CMOS</td>
</tr>
</tbody>
</table>

Averaging networks designed to reduce input referred offset by 3x
OFFSET CALIBRATION

S. Sutardja, "360 Mb/s (400 MHz) 1.1 W 0.35μm CMOS PRML read channels with 6 burst 8-20× over-sampling digital servo," ISSCC Dig. Techn. Papers, Feb. 1999.
COMPARATOR WITH OFFSET CORRECTING DAC

HIGH-PERFORMANCE FLASH WITH CALIBRATION (1)

[Park & Flynn, "A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS," CICC 2006]
COMPARATOR REDUNDANCY (1)

- Idea: Build a "sea of imprecise comparators", then determine which ones to use...

COMPARATOR REDUNDANCY (2)

Paulus et al., "A 4GS/s 6b flash ADC in 0.13um CMOS," VLSI Circuits Symposium, 2004
STOCHASTIC FLASH ADC

- Fully synthesized ADC using ‘digital’ comparator cells (large offsets)
- Use more than 1 comparator for a reference threshold
  - Use ‘detection theory’ to make accurate decisions around a threshold, by using more than one observation
- Low speed designs (<20 MS/s)

A 6b Stochastic Flash Analog-to-Digital Converter Without Calibration or Reference Ladder

[Authors: Silver Weaver², Benjamin Hershbren², Daniel Kristin³, and Un-Ku Moon⁴]
FLASH ADC: CASE STUDY
A Distortion Compensating Flash Analog-to-Digital Conversion Technique

Venkata Srinivas, Shanthi Pavan, Ashish Lachhwani, and Naga Sasidhar
Fig. 2. Flash ADC behavior with an ideal track-and-hold.

Fig. 3. Flash ADC behavior with a real track-and-hold having static nonlinearity.
PRE-DISTORTED REFERENCES

Fig. 5. ADC output spectrum with track-and-hold having static nonlinearity with (a) linear references and (b) predistorted references.
ADC ARCHITECTURE
T/H CIRCUIT
COMPARATOR

Schematic of the preamplifier.
NON-LINEAR REFERENCE GENERATOR

Fig. 13. Linear reference generator.

ADC TESTING

Fig. 19. Normalized output spectrum of the ADC.

Fig. 20. Illustration of (a) continuous background noise mode and (b) discontinuous background noise mode.
TEST RESULTS

Figure of Merit

\[
\text{Figure of Merit} = \frac{\text{Energy}}{(\text{conversion\_step})} = \frac{P_{\text{diss}}}{2^{\text{ENOB}} \times f_{\text{samp}}}
\]

<table>
<thead>
<tr>
<th>Summary of ADC Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>Nominal input swing</td>
</tr>
<tr>
<td>DNL (nominal input range)</td>
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<tr>
<td>INL (nominal input range)</td>
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<tr>
<td>SNDR</td>
</tr>
<tr>
<td></td>
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<tr>
<td>Power consumption</td>
</tr>
<tr>
<td>Active Area</td>
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<tr>
<td>Chip package</td>
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</table>
REFERENCES


3. Y. Chiu, Data Converters Lecture Slides, UT Dallas 2012.