DAC Architectures

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Static Performance of DACs
DAC Transfer Characteristics

Note: \( V_{out} (b_i = 1, \text{ for all } i) = V_{FS} - \Delta = V_{FS}(1 - 2^{-N}) \neq V_{FS} \)

- \( N \) = number of bits
- \( V_{FS} \) = full-scale range
- \( \Delta = V_{FS}/2^N = 1\text{ LSB} \)
- \( b_i = 0 \) or 1
Ideal DAC Transfer Curve

- $V_{FS} - \Delta$
- $V_{FS}/2$
- $V_{out}$
- $D_{in}$

Points at $D_{in}$: 000, 001, 010, 011, 100, 101, 110, 111
Offset

\[ V_{\text{out}} \]

\[ V_{\text{FS}} - \Delta \]

\[ \frac{V_{\text{FS}}}{2} \]

\[ V_{\text{os}} \]

\[ D_{\text{in}} \]
Gain Error

\[ V_{\text{out}} \]

\[ V_{\text{FS}} - \Delta \]

\[ \frac{V_{\text{FS}}}{2} \]

\[ D_{\text{in}} \]

Points:
- 000
- 001
- 010
- 011
- 100
- 101
- 110
- 111
Monotonicity

The diagram illustrates the monotonic behavior of a system with inputs $D_{in}$ and outputs $V_{out}$. The axes represent $V_{FS-\Delta}$, $V_{FS}/2$, and $D_{in}$, with discrete input values from 000 to 111. The graph shows a clear increasing trend, indicating a monotonic relationship between the input and output signals.
Differential and Integral Nonlinearities

- DNL = deviation of an output step from 1 LSB \( (= \Delta = \frac{V_{FS}}{2^N}) \)
- INL = deviation of the output from the ideal transfer curve

\[
DNL_i = \frac{i^{\text{th}} \text{ Step Size} - \Delta}{\Delta}
\]
INL = cumulative sum of DNL

\[ \text{INL}_i = \sum_{j=0}^{i} \text{DNL}_j \]
DNL and INL

- DNL measures the uniformity of quantization steps, or incremental (local) nonlinearity; small input signals are sensitive to DNL.
- INL measures the overall, or cumulative (global) nonlinearity; large input signals are often sensitive to both INL (HD) and DNL (QE).
Endpoints of the transfer characteristic are always at 0 and $V_{FS-\Delta}$
Measure DNL and INL (Method II)

Endpoints of the transfer characteristic may not be at 0 and $V_{FS-\Delta}$
Measure DNL and INL

Method I (endpoint stretch)

\[ \Sigma(\text{INL}) \neq 0 \]

Method II (LS fit & stretch)

\[ \Sigma(\text{INL}) = 0 \]
DAC Architecture

- **Nyquist DAC architectures**
  - Binary-weighted DAC
  - Unit-element (or thermometer-coded) DAC
  - Segmented DAC
  - Resistor-string, current-steering, charge-redistribution DACs

- **Oversampling DAC**
  - Oversampling performed in digital domain (zero stuffing)
  - Digital noise shaping (ΣΔ modulator)
  - 1-bit DAC can be used
  - Analog reconstruction/smoothing filter
Binary-Weighted DAC
Binary-Weighted CR DAC

\[ C_u = \text{unit capacitance} \]

- Binary-weighted capacitor array → most efficient architecture
- Bottom plate @ \( V_R \) with \( b_j = 1 \) and @ GND with \( b_j = 0 \)
Binary-Weighted CR DAC

\[
V_o = \left( \frac{2^N C_u}{C_p + 2^N C_u} \right) \cdot V_R \cdot \sum_{j=1}^{N} b_{N-j} \cdot \frac{2^{-j} C_u}{2^j}
\]

- \( C_p \rightarrow \) gain error (nonlinearity if \( C_p \) is nonlinear)
- INL and DNL limited by capacitor array mismatch
Stray-Insensitive CR DAC

\[ V_o = \left( \frac{2^N C_u}{2^N C_u + \frac{C_p + 2^{N+1} C_u - C_u}{A}} \right) \cdot V_R \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j} \]

Large \( A \) needed to attenuate summing-node charge sharing
MSB Transition

\[ V_o(0111) = \left( \frac{C_1 + C_2 + C_3}{C_p + C + \sum_{j=1}^{4} 2^{4-j} C} \right) \cdot V_R \]

\[ V_o(1000) = \left( \frac{C_4}{C_p + C + \sum_{j=1}^{4} 2^{4-j} C} \right) \cdot V_R \]

Assume: \( C_4 - (C_1 + C_2 + C_3) = C_u + \delta C \),

\[ \text{DNL} = \left[ V_o(1000) - V_o(0111) - 1\text{LSB} \right] / 1\text{LSB} \]

\[ = \frac{\delta C}{\sum C} / \frac{C_u}{\sum C} = \delta C / C_u \]

Largest DNL error occurs at the midpoint where MSB transitions, determined by the mismatch between the MSB capacitor and the rest of the array.
\( \delta C > 0 \) results in positive DNL

\( \delta C < 0 \) results in negative DNL or even nonmonotonicity
Output Glitches

- Glitches cause waveform distortion, spurs and elevated noise floors
- High-speed DAC output is often followed by a de-glitching SHA

- Cause: Signal and clock skew in circuits
- Especially severe at MSB transition where all bits are switching – 0111…111 → 1000…000
SHA samples the output of the DAC after it settles and then hold it for $T$, removing the glitching energy.

SHA output must be smooth (exponential settling can be viewed as pulse shaping $\rightarrow$ SHA BW does not have to be excessively large).
Frequency Response

\[ |H(f)| \]

\[ f \]

\[ 0 \]

\[ f_s \]

\[ 2f_s \]

\[ 3f_s \]

\[ f \]

\[ H_zoh(j\omega) = e^{-\frac{j\omega T}{2}} \cdot \frac{\sin\left(\frac{\omega T}{2}\right)}{\omega T / 2} \]

\[ H_{sha}(j\omega) = \frac{1}{1 + j\omega / \omega_{-3dB}} \]
Binary-Weighted Current-Steering DAC

\[ V_o = IR \cdot \sum_{j=1}^{N} \frac{b_{N-j}}{2^j} \]

- Current switching is simple and fast
- \( V_o \) depends on \( R_{out} \) of current sources without op-amp
- INL and DNL depend on matching, not inherently monotonic
- Large component spread \( (2^{N-1}:1) \)
R-2R DAC

- A binary-weighted current DAC
- Component spread greatly reduced (2:1)
Unit-Element DAC
Resistor-String DAC

- Simple, inherently monotonic → good DNL performance
- Complexity ↑ speed ↓ for large N, typically N ≤ 8 bits
Code-Dependent $R_0$

- $R_0$ of ladder varies with signal (code)
- On-resistance of switches depend on tap voltage

Signal-dependent $R_0C_0$ causes HD
DNL

\[ \Delta R = [0, \sigma_R] \]

\[
V_j = \frac{1}{N} \sum_{k=1}^{j-1} R_k \cdot V_R = \frac{(j-1)R + \sum_{k=1}^{j-1} \Delta R_k}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R
\]

\[
V_{j-1} = \frac{(j-2)R + \sum_{k=1}^{j-2} \Delta R_k}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R
\]

\[
V_j - V_{j-1} = \frac{R + \Delta R_{j-1}}{NR + \sum_{1}^{N} \Delta R_k} \cdot V_R \approx \frac{V_R}{N} + \frac{\Delta R_{j-1}}{NR} \cdot V_R
\]

\[
\text{DNL}_j = \left( V_j - V_{j-1} - \frac{V_R}{N} \right) / \frac{V_R}{N} \approx \frac{\Delta R_{j-1}}{R} \Rightarrow \text{DNL} = 0, \sigma_{\text{DNL}} = \frac{\sigma_R}{R}
\]
\[ V_j = \frac{\sum_{k=1}^{j-1} R_k}{\sum_{k=1}^{N} R_k} \cdot V_R = \frac{(j-1)R + \sum_{k=1}^{j-1} \Delta R_k}{NR + \sum_{k=1}^{N} \Delta R_k} \cdot V_R \approx \frac{j-1}{N} V_R + \frac{(N-j+1)\sum_{k=1}^{j-1} \Delta R_k - (j-1)\sum_{k=j}^{N} \Delta R_k}{N^2R} V_R \]

\[ \Rightarrow \overline{V_j} = \frac{j-1}{N} V_R, \quad \sigma_{V_j}^2 \approx \frac{(j-1)(N-j+1)}{N^3} \frac{\sigma_R^2}{R^2} V_R^2 \]

\[ \Rightarrow \sigma_{V_j}^2 (\text{max}) \approx \frac{1}{4N} \frac{\sigma_R^2}{R^2} V_R^2, \quad \text{when} \quad j = \frac{N}{2} + 1 \approx \frac{N}{2} \]

\[ \text{INL}_j = \left( V_j - \frac{j-1}{N} V_R \right) / \frac{V_R}{N} \Rightarrow \overline{\text{INL}} = 0, \quad \sigma_{\text{INL}} (\text{max}) \approx \frac{\sqrt{N}}{2} \left( \frac{\sigma_R}{R} \right) \]
INL and DNL of Binary-Wtd DAC

A Binary Weighted DAC is typically constructed using unit elements, the same way as that of a Unit Element DAC, for good component matching accuracy.

\[
\text{INL} = 0, \quad \sigma_{\text{INL}}(\text{max}) \approx \frac{\sqrt{N}}{2} \left( \frac{\sigma_R}{R} \right) \\
\Rightarrow \quad \text{DNL} = 0, \quad \sigma_{\text{DNL}}(\text{max}) = 2 \cdot \text{INL} \approx \sqrt{N} \left( \frac{\sigma_R}{R} \right)
\]
Current-Steering DAC

- Fast, inherently monotonic → good DNL performance
- Complexity increases for large N, requires B2T decoder
Unit Current Cell

- $2^N$ current cells typically decomposed into a $(2^{N/2} \times 2^{N/2})$ matrix
- Current source cascoded to improve accuracy ($R_o$ effect)
- Coupled inverters improve synchronization of current switches
Segmented DAC
**Binary-weighted DAC**

- **Pros**
  - Min. # of switched elements
  - Simple and fast
  - Compact and efficient

- **Cons**
  - Large DNL and glitches
  - Monotonicity not guaranteed

- **INL/DNL**
  - $\text{INL}(\text{max}) \approx (\sqrt{N}/2)\sigma$
  - $\text{DNL}(\text{max}) \approx 2\times \text{INL}$

**Unit-element DAC**

- **Pros**
  - Good DNL, small glitches
  - Linear glitch energy
  - Guaranteed monotonic

- **Cons**
  - Needs B2T decoder
  - complex for $N \geq 8$

- **INL/DNL**
  - $\text{INL}(\text{max}) \approx (\sqrt{N}/2)\sigma$
  - $\text{DNL}(\text{max}) \approx \sigma$

Combine BW and UE architectures → Segmentation
Segmented DAC

- MSB DAC: M-bit UE DAC
- LSB DAC: L-bit BW DAC
- Resolution: $N = M + L$
- $2^{M+L}$ switching elements
- Good DNL
- Small glitches
- Same INL as BW or UE
**Example**: $N = 12$, $M = 8$, $L = 4$, $\sigma = 1\%$

<table>
<thead>
<tr>
<th>Architecture</th>
<th>$\sigma_{\text{INL}}$</th>
<th>$\sigma_{\text{DNL}}$</th>
<th># of s.e.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit-element</td>
<td>0.32 LSB’s</td>
<td>0.01 LSB’s</td>
<td>$2^N = 4096$</td>
</tr>
<tr>
<td>Binary-weighted</td>
<td>0.32 LSB’s</td>
<td>0.64 LSB’s</td>
<td>$N = 12$</td>
</tr>
<tr>
<td>Segmented</td>
<td>0.32 LSB’s</td>
<td>0.06 LSB’s</td>
<td>$2^M+L = 260$</td>
</tr>
</tbody>
</table>

Max. DNL error occurs at the transitions of MSB segments
Example: “8+2” Segmented Current DAC

Common-centroid global biasing + divided 4 quadrants of current cells
MSB-DAC Biasing Scheme

Chip A: Merged 4 quadrants

Chip B: Separated 4 quadrants

DNL = 0.2 LSB

DNL = 0.1 LSB
Randomization and Dummies

- Column and row randomization to improve INL

- Diagram with symbols for dummy-cells and active-cells:
Current-Steering DAC Unit Cell
Current-Steering DAC Calibration
References

1. **Y. Chiu, Data Converters Lecture Slides, UT Dallas 2012.**
   - K. Khanoyan, F. Behbahani, A. A. Abidi, VLSI, 1999, pp. 73-76.
   - G. A. M. Van Der Plas et al., JSSC, pp. 1708-1718, issue 12, 1999.